

10

```
FOR (i=0; i<2; i=i+1)
  begin
    out[i] = 8'b10101010;
    enable[i] = up[2*i];
  end
```

FIGURE 1

```
reg y [3:0];
WHILE (x <= y)
begin
    fpl_bit[x+y] = mm_iru[x-y];
end
```



FIGURE 2

```
16    18    20    14
      ↓    ↓    ↓    ↗
FOR (INIT; EXIT; INC)
begin
    BODY_OF_STATEMENTS;
end
      ↗    ↗
      22
```

FIGURE 3

```
out[0] = 8'b10101010;  
enable[0] = ~up[0]; } 24  
  
out[0] = 8'b10101010;  
enable[0] = ~up[2]; }
```

FIGURE 4

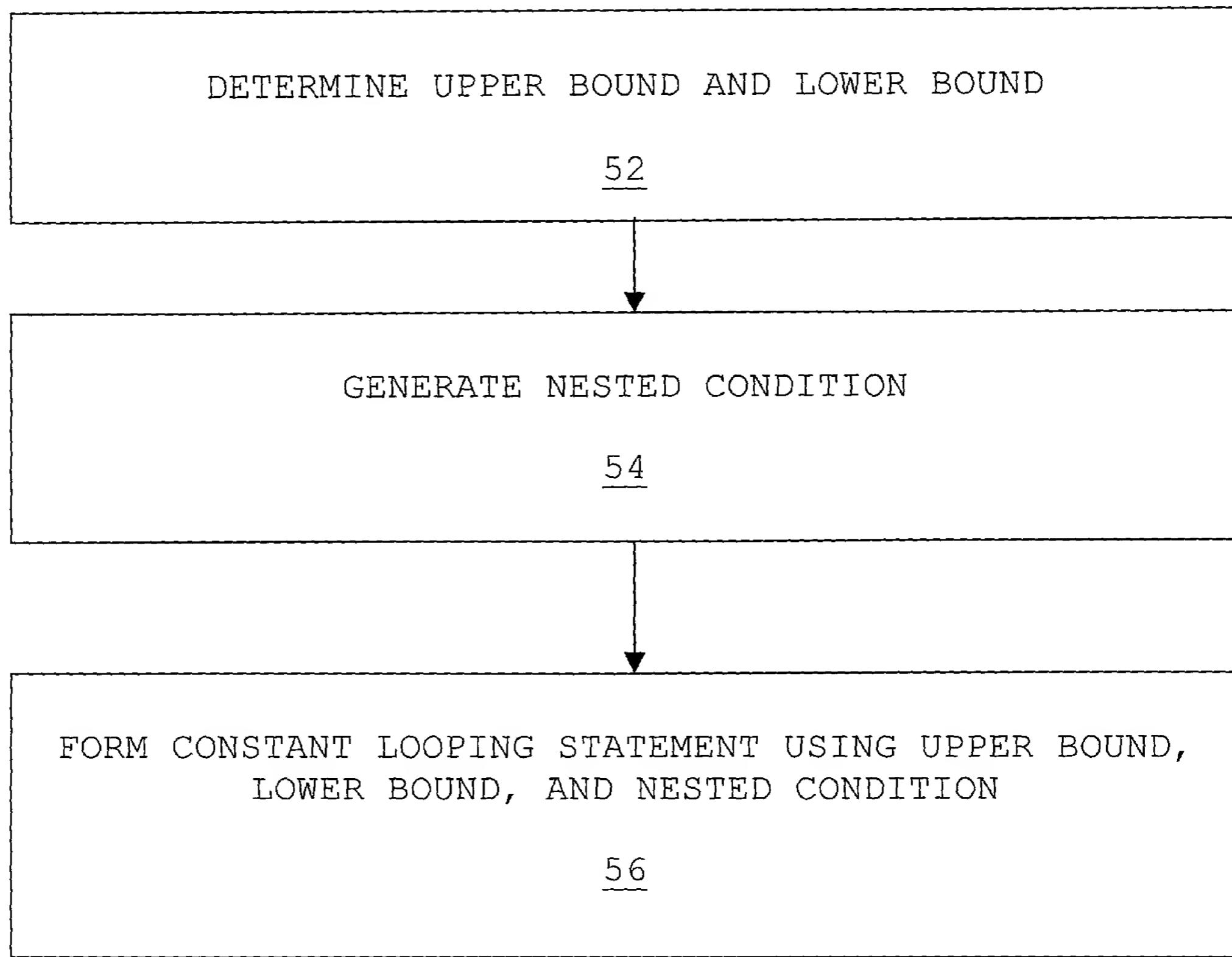


FIGURE 5

60 } FOR (LOWER_BOUND_EXPRESSION; UPPER_BOUND_EXPRESSION;
61 } INCREMENT_EXPRESSION) 66
62 } if (INIT && EXIT) 68
63 } STATEMENT_BODY 69

FIGURE 6

80
82 ` reg i [3:0];
84 ` reg j [1:0]; 74
84 ` reg k [2:0]; 76
70 { for (j<=i; i<k; i=i+1)
72 statement_body 78

FIGURE 7

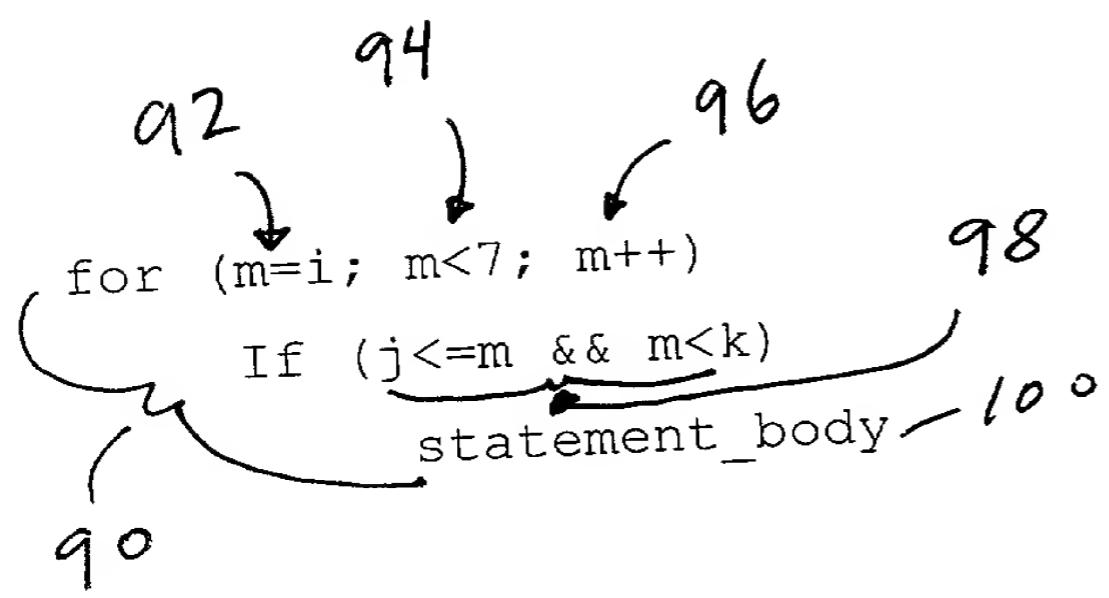


FIGURE 8

```
112
WHILE ( x <= 15 )
  if ( x <= y ) 114
    begin
      fpl_bit[x+y] = mm_iru[x-y];
    end
  110
```

116

FIGURE 9